Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A ~~linear scalable~~ method of processing a digital signal ~~under control of instructions executing on a multiprocessor computing system~~ by computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) of the digital signal, ~~signal using a decimation in time approach,~~ the method comprising using a multiprocessor computing system having a plurality of processors P to perform the steps of:

computing an N-point FFT/IFFT of the signal using ~~a first plurality~~ first and second sets of butterfly computational stages, each stage in the ~~first plurality of~~ second set of stages employing a plurality of butterfly ~~operations having a first radix,~~ operations, wherein each of the butterfly operations in each stage in the ~~first plurality~~ second set of stages has a single, un-nested computation loop; and ~~loop of the first radix;~~

distributing the plurality of butterfly operations in each stage of the ~~first plurality~~ second set of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency among the parallel processors. ~~in the stage; and~~

~~storing the transformed signal in a memory.~~

2. (Currently Amended) A ~~linear scalable~~ method as claimed in claim 1 wherein said step of distributing butterfly operations in each stage is implemented by assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor.

3. (Currently Amended) A ~~linear scalable~~ multiprocessor system to process a digital signal by computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) of the signal ~~in a multiprocessing system~~ using a decimation in time or decimation in frequency approach, comprising:

the multiprocessor system having a plurality of processors P and configured to implement:

means for computing a first plurality of $\log_2 P$ stages of an N-point FFT/IFFT of the signal;

means for computing a second plurality of stages of ~~an~~ the N-point FFT/IFFT of the signal using in each stage of the second plurality of stages a plurality of butterfly operations, wherein each butterfly operation employs a single butterfly computation loop ~~of a first radix and~~ without employing nested loops; and

means for distributing the butterfly operations in each stage of the second plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stages of the second plurality of stages. ~~stage; and~~

~~a memory for storing inputs and output of the means for computing.~~

4. (Currently Amended) A ~~linear scalable~~ system as claimed in claim 3 wherein said means for distributing the butterfly operations is implemented by means for assigning to each processor of the multi-processor system respective addresses of memory locations in the means for storing inputs and outputs corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor.

5. (Currently Amended) A computer-readable ~~memory~~ storage medium whose contents cause a system having a plurality of processors to perform a linear scalable method of transforming a signal by computing with the plurality of processors a Fast Fourier Transform (FFT) or an Inverse Fast Fourier Transform (IFFT) of the ~~signal using a decimation in time approach,~~ signal, the method comprising:

computing a first plurality of ~~first and second stages of $\log_2$N~~ stages of an N-point FFT/IFFT; and

computing a second plurality of stages of the N-point FFT ~~as a single radix-4 butterfly operation while implementing the remaining ($\log_2$N-2) stages using radix-2 butterfly operations, wherein each radix-2 butterfly operation employs a single radix-2 butterfly computation loop~~ without employing nested ~~loops;~~ loops and by distributing the butterfly operations in each stage of the second plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage. ~~stage; and~~

~~storing the transformed signal in a memory.~~

6. (Currently Amended) The computer computer-readable ~~memory~~ storage medium of claim 5 wherein distributing the butterfly operations comprises assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor.

7. (Currently Amended) The method of claim 1 wherein the second plurality of butterfly operations have ~~first radix is~~ a radix-2 radix.

8.-10. (Canceled)

11. (Previously Presented) The method of claim 2, wherein the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location.

12. (Currently Amended) The system of claim 3 wherein the second plurality of stages have ~~first radix is~~ a radix-2 radix.

13. (Currently Amended) The system of claim 12 wherein the second plurality of stages comprises $\log_2 N$-2 stages, further comprising computing a first and second stage of $\log_2 N$ stages of the N-point FFT/IFFT as a single radix-4 butterfly operation.

14. (Canceled)

15. (Previously Presented) The system of claim 4 wherein the means for assigning is configured to insert a binary digit in an address of a memory location.

16. (Currently Amended) A computer-readable ~~memory~~ storage medium whose contents cause a system having a plurality of processors to perform a linear scalable method of transforming a signal, the method comprising:

computing an N-point FFT/IFFT using a first plurality of butterfly computational stages and a second plurality of butterfly computational stages, each stage in the ~~first~~ second plurality of stages employing a plurality of butterfly operations having ~~a first radix, wherein each of the butterfly operations in each stage of the first plurality of stages has~~ a single, un-nested computation ~~loop of the first radix;~~ loop; and

distributing the plurality of butterfly operations in each stage of the ~~first~~ second plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage. ~~stage; and~~

~~storing the transformed signal in a memory.~~

17. (Currently Amended) The computer-readable ~~memory~~ storage medium of claim 16 wherein the distributing butterfly operations in each stage comprises assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor.

18. (Currently Amended) The computer-readable ~~memory~~ storage medium of claim 17 wherein the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location.

19-26. (Canceled)

27. (Currently Amended) A method of transforming a digital signal, the method comprising:

using a multiprocessor computing system having a plurality P of processors to:

~~computing, with a multiprocessor computing system having a plurality of processors P,~~ compute a first number of butterfly stages of an N-point Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT); and

~~computing~~ compute remaining butterfly stages of the N-point FFT/IFFT with a single iterative loop wherein each processor computes an equal number of butterfly ~~operation in each stage of a loop iteration is computed on a single respective processor in the plurality of processors~~ operations and there is no data dependency between butterflies in a stage of an iteration of the loop. ~~loop; and~~

~~storing the transformed digital signal in a memory medium.~~

28. (Previously Presented) The method of claim 27 wherein the plurality of processors comprises two processors and the first number of butterfly stages consists of one stage.

29. (Previously Presented) The method of claim 27 wherein the plurality of processors comprises four processors and the first number of butterfly stages consists of two stages.

30. (Canceled)

31. (Currently Amended) A system, comprising:

an instruction fetch cache; and

a plurality ~~P~~ of processors P coupled to the instruction fetch catch and configured to:

compute a first number of butterfly stages of an N-point Fast Fourier Transform (FFT) or Inverse Fast Fourier Transform (IFFT) of a digital signal; and

compute remaining butterfly stages of the N-point FFT/IFFT with a single iterative loop wherein ~~each butterfly operation in each stage of a loop iteration is computed on a single respective processor in the plurality of processors and~~ there is no data dependency between butterflies in a stage of an iteration of the loop.

32. (Previously Presented) The system of claim 31 wherein the plurality of processors comprises two processors and the first number of butterfly stages consists of one stage.

33. (Previously Presented) The system of claim 31 wherein the plurality of processors comprises four processors and the first number of butterfly stages consists of two stages.

34. (Canceled)